

What is claimed is:

1           1. A method of testing a semiconductor device having a memory, comprising:  
2                 selecting a portion of said memory;  
3                 testing said selected portion of said memory;  
4                 designating said selected portion of said memory as a designated memory  
5           in response to an acceptable testing result; and  
6                 storing data in said designated portion of said memory for retrieval at a  
7           later time.

1           2. The method of claim 1, further including attempting a soft repair of said  
2   selected memory portion in response to an unacceptable test result and designating said  
3   selected portion of memory in response to a successful repair.

1           3. The method of claim 2, further including selecting and testing additional  
2   memory portions of said memory in response to an unacceptable test result and  
3   unsuccessful repair attempt until a portion of said memory having an acceptable test  
4   result or successful repair is found.

1           4. The method of claim 1, wherein said selected portion of memory is selected to  
2   have a sufficient word length and number of bits for storing said data.

1 5. The method of claim 1, further including compressing said data before storing  
2 said data in said designated portion of said memory.

1 6. The method of claim 5, further including decompressing said data after  
2 retrieving said data from said designated portion of said memory.

1 7. The method of claim 1, wherein said data comprises bitmaps, memory fail data,  
2 LBIST pass/fail signatures or pass/fail data.

1 8. The method of claim 1, further including sending said data to a tester.

1 9. The method of claim 1, wherein said data is generated by ABIST or LBIST.

1 10. A method of testing a semiconductor device having a memory, comprising:  
2 providing a designated memory;  
3 performing ABIST on a memory segment to generate memory test data;  
4 storing said memory test data in said designated memory; and  
5 retrieving said test data at a later time.

1 11. The method of claim 10, wherein said memory test data is a bitmap.

1           12. The method of claim 10, wherein said memory test data is fail data generated  
2    from a bitmap.

1           13. The method of claim 12, further including ORing additional test data with  
2    said test data already stored in said designated memory.

1           14. The method of claim 10, further including compressing said data before  
2    storing said data in said designated memory.

1           15. The method of claim 14, further including decompressing said data after  
2    retrieving said data from said designated memory.

1           16. A method of testing a semiconductor device having a memory, comprising:  
2                providing a designated memory;  
3                performing an LBIST on a device logic function to generate a set of  
4    LBIST signatures;  
5                storing said LBIST signatures in said designated memory; and  
6                retrieving said LBIST signatures at a later time.

1           17. The method of claim 16, further including compressing said data before  
2    storing said data in said designated memory.

1 18. The method of claim 17, further including decompressing said data after  
2 retrieving said data from said designated memory.

1 19. The method of claim 16, wherein said LBIST is run on every group of N  
patterns, each group of N patterns having a cumulative fail signature.

1 20. The method of claim 19, further including :  
2 identifying a failing group of N patterns;  
3 performing a second LBIST on said device logic functions using every LBIST  
4 pattern from said group of N patterns; and  
5 identifying every failing pattern in said group of N patterns.

1 21. A method of testing a function of a semiconductor device having a memory,  
2 comprising:  
3 providing a designated memory;  
4 performing a first test using a test pattern in a first corner of the test  
5 specification of said function of said semiconductor device ;  
6 storing the result of said first test in said designated memory;  
7 performing a second test using said test pattern in a second corner of the  
8 test specification of said function of said semiconductor device;  
9 retrieving said first test result from said designated memory; and  
10 comparing said first test result with said second test result.

1           22. The method of claim 21, further including generating a pass signal in response  
2 to said first test result matching said second test result and generating a fail signal in  
3 response to said first test result not matching said second test result.

1           23. The method of claim 21 further including compressing said first test result  
2 before storing said first test result in said designated memory and decompressing said  
3 first test result after retrieving said first test result from said designated memory but  
4 before comparing said first test result to said second test result.

1           24. The method of claim 21 wherein said designated memory contains at least as  
2 many bits as there are latches in said function of said semiconductor device.

1           25. The method of claim 24, wherein said designated memory has a word length  
2 at least equal to the number of scan chains in said function of said semiconductor device.

1           26. A semiconductor device comprising:  
2                 a memory;  
3                 an ABIST engine adapted to test said memory; and  
4                 an interface adapted to send test data to and receive test data from a  
5                 designated portion of said memory.

1           27. The semiconductor device of claim 26, wherein said interface is an ABIST  
2 interface and said test data is bitmap data.

1           28. The semiconductor device of claim 27, wherein said ABIST interface includes  
a data compress function and said ABIST engine includes a data decompress function.

1           29. The semiconductor device of claim 26, further including an LBIST engine  
2 adapted to test device logic functions and wherein said interface is an LBIST interface  
3 and said test data comprises LBIST patterns.

1           30. The semiconductor device of claim 29, wherein said LBIST interface includes  
2 a data compress function and said LBIST engine includes a data decompress function.

1           31. The semiconductor device of claim 26, further including a corner compare  
2 function adapted to compare the results of a test pattern run in two corners of the test  
3 specification of said semiconductor device and wherein said interface is a corner  
4 interface and said test data is the result of a first corner test.

1           32. The semiconductor device of claim 31, wherein said corner interface includes  
2 a data compress function and said corner compare includes a data decompress function.

1           33. The semiconductor device of claim 26, further including a repair function  
adapted to soft repair said designated portion of said memory segment.